REMARKS

Claims 1-22 are pending in the application.

Claim Rejections – 35 U.S.C. § 103

(a) Claims 2-7, 10-15, and 18-21 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Rabeler (USP 6,594,746) and Bandoo (USP 3,803,559). This rejection is respectfully traversed. Claims 2 and 18 are independent.

The Examiner contends that Rabeler discloses all elements of claim 2 except for:

(1) A monitor flag indicating that a specified address space is being accessed;

(2) An access permission setting register for setting whether or not an access with respect to an address other than the address range should be permitted;

(3) Memory Access is controlled based on the content of the access permission setting access register; and

(4) Indicating that a predetermined address space is being accessed based on an address bus signal and an instruction read out signal indicative of a first cycle of an instruction.

However, the Examiner cites Bandoo as allegedly teaching an access permission setting register, and cites Bournas as allegedly teaching that an indication that a predetermined address space is being accessed in based on an address bus signal and instruction read out signal indicative of a first cycle of an instruction. Applicants respectfully disagree.

Firstly, it is pointed out that the Examiner's rejection is contradictory. Specifically, the Examiner states in page 3, lines 13-18, of the instant Office Action that Rabeler does not teach a

monitor flag, but then implies in page 5, lines 16-19, that Rabeler may include a monitor flag. Applicant cannot ascertain whether or not the Examiner is contending that Rabeler does or does not teach a monitor flag. Further, such an inconsistency does not clearly set forth which element of Rabeler the Examiner contends is a monitor flag.

It is respectfully submitted that this inconsistency does not provide Applicants a fair opportunity to respond to the outstanding rejections, and for this reason, a new Office Action clearly setting out that Examiner's position regarding this element should be issued. Otherwise, if strictly construing the wording of the Office Action as it currently reads, Applicants submit that the Examiner's combination of Rabeler, Bandoo, and Bournas fails to teach the monitor flag, and hence claim 2 is allowable.

The above notwithstanding, in a sincere effort to further prosecute and expedite allowance of the present application, the following arguments are further submitted. The following arguments assume that the Examiner is referring to the "mode bit" of Rabeler as a monitor flag. It is, however, expressly submitted at this juncture that such an assumption is solely for the purpose of furthering prosecution of the present application, and is not in any way an admission, of any form, on the Applicants' part. Applicants explicitly point out that the following assumptions are necessary as a result of the Examiner's contradictory statements in the outstanding Office Action. If the following assumptions are inaccurate, the Examiner is respectfully requested to issue a new Office Action, clearly outlining the Examiner's position with regard to the monitor flag, such that assumptions by Applicants is unnecessary.

Assuming that the Examiner is referring to the mode bit of Rebeler as being a monitor flag, it is pointed out that the Examiner's combination still fails to render obvious the invention of claim 2.

Claim 2 requires that the monitor flag toggles a flag based on an address bus signal and an instruction read out signal indicative of a first cycle of an instruction. In contrast, the mode bit of Rabeler is set by performing an explicit jump instruction (see, col. 4, lines 15-18). The difference between claim 2 and Rabeler in this regard can be viewed as the former being reactive, whilst the latter being proactive. That is, in the invention of claim 2, the monitor flag toggles a flag based on a certain condition (e.g., address bus signal and instruction read out signal), and on the other hand, Rabeler actively performs a special jump instruction to set the mode bit. Setting of the mode bit in Rabeler is not a reaction to a certain condition being satisfied, rather, it is itself the initiating action.

Due to the Examiner's contradictory statements in the instant Office Action, it is not clear if the Examiner recognizes this difference between claim 2 and Rabeler. However, it is noted that the Examiner refers to Bournas to allegedly teach the feature of providing an indication that a predetermined address space is being accessed based on an address bus signal and an instruction read out signal. For the purposes of furthering prosecution, it is assumed that the Examiner is suggesting that one would combine/replace the special jump instruction of Rabeler with the determination process of Bournas, as an alternative way to set the mode bit of Rabeler.

It is firstly submitted that such a combination of Bournas and Rabeler lacks motivation, and appears to be based on improper hindsight. The Examiner states that one would perform the above combination in order to maintain high security level in the chip card. However, it is

pointed out that Rabeler already achieves the same effect of high security. In fact the very component that the Examiner is suggesting to replace is a key element of Rabeler that provides this same effect of high security. In view of this, it is submitted that one of ordinary skill in the art therefore would not be motivated to use the arrangement of Bournas over that of Rabeler, as such a combination results in no additional advantage or effect. The Examiner has not attempted to suggest that Bournas provides any better or higher security than Rabeler.

Next, it is respectfully submitted that the Examiner has incorrectly characterized the teaching of Bournas. Referring to col. 6, lines 23-66, it is submitted that this portion of Bournas (which the Examiner relies upon) does not in fact teach or suggest "*toggling a flag . . . based on an address bus signal and an instruction read out signal . . .*" as recited in claim 2. Rather, this portion of Bournas describes the process in which Read (R), Write (W), and Erasure (E) commands are permitted or inhibited from being passed onto a memory. There is not suggestion that this process is for toggling a flag indicating that a predetermined address space is being accessed.

In view of the above, it is submitted that the Examiner's combination even more so lacks motivation. Specifically, there is no suggestion that the above process of Bournas should be used to toggle a flag. Even more specifically, there is no suggestion that the above process of Bournas should replace the special jump instruction of Rabeler, as the means for setting the mode bit.

Claim 2, and the claims dependent therefrom, are hence submitted to be novel and inventive over the combination of Rabeler, Bandoo, and Bournas. Similar arguments are equally applicable to independent claim 18, and the claims dependent therefrom.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

(b) Claims 1, 9, and 17 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Rabeler and Bandoo and Sakaki (EP 0,735,488). This rejection is respectfully traversed. Claims 1 and 17 are independent.

The invention of claim 1 pertains to the description in page 13, lines 18-25 of the specification. That is, the invention of claim 1 determines if a system software (which is stored in a specified address space) is being executed, and if so, outputs a writing reference signal when this system software attempts to perform a writing operation. The outputted writing reference signal serves as an indication indicating that this writing operation is permitted to write to protected registers.

As acknowledged by the Examiner in the Office Action, both Rabeler and Bandoo fails to disclose or suggest the "register writing control means," as recited in claim 1.

Sakaki discloses, in col. 2, lines 36-39, setting a disable area that inhibits accessing of another program.

Sakaki, however, does not determine "whether a writing operation occurs from a predetermined address space or from an address space other than the predetermined address space." Accordingly, Sakaki fails to disclose or suggest the "register writing control means" as recited in claim 1.

Therefore, the references, taken singly or in combination, fail to disclose or suggest the "register writing control means" as recited in claim 1.

Claim 9, dependent on claim 1, is allowable at least for its dependency on claim 1.

Claim 17 is allowable at least for the similar reasons as stated in the foregoing with respect to claim 1.

The Examiner is respectfully requested to reconsider and withdraw this rejection.

(c) Claims 8, 16, and 22 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Rabeler and Bandoo and Bournas (USP 5,452,). This rejection is respectfully traversed.

Claims 8 and 16, variously dependent on claim 2, are allowable at least for their dependency on claim 2.

Claim 22, indirectly dependent on claim 18, is allowable at least for its dependency on claim 1.

The Examiner is respectfully requested to reconsider and withdraw this rejection.

Conclusion

Accordingly, in view of the above amendments and remarks, reconsideration of the rejections and allowance of the pending claims in the present application are respectfully requested.

The Examiner is respectfully requested to enter this Reply After Final in that it raises no new issues. Alternatively, the Examiner is respectfully requested to enter this Reply After Final in that it places the application in better form for Appeal.

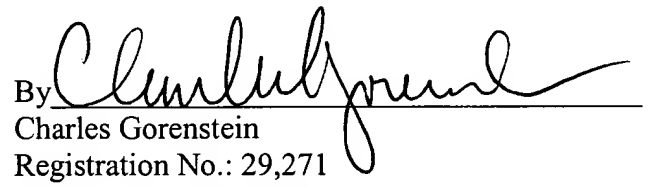
Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Maki Hatsumi (#40,417) at the

telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or to credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Dated: April 3, 2006

Respectfully submitted,

By 

Charles Gorenstein
Registration No.: 29,271
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
P.O. Box 747
Falls Church, Virginia 22040-0747
(703) 205-8000
Attorney for Applicant